**ECE 329**

**Digital Circuit Design II+Lab.**

**Fall 2018/2019**

**LAB # 4**

 **15.10.2018**

**Objective:**

To learn about asynchronous counters

1. **Using T Flip Flops in Design**
2. **Using JK Flip Flops in design**
3. **Designing Synchronous Counters**
4. **Design a 3 bit synchronous up counter by using JK flip flops**

**Procedure:**

1. Fill the state transition table for a 3 bit synchronous up counter
2. Make K-maps from this table
3. Design your circuit from the results obtained in step 2
4. Simulate your circuit on ORCAD, make comments on the output, is it what you have expected?
5. **Design a 3 bit synchronous down counter by using JK flip flops**

**Procedure:**

1. Fill the state transition table for a 3 bit synchronous down counter,
2. Make K-maps from this table,
3. Design your circuit from the results obtained in step 2,
4. Simulate your circuit on ORCAD, make comments on the output, is it what you have expected?
5. **Design a 4 bit synchronous up counter by using T flip flops**

**Procedure:**

1. Fill the state transition table for a 4 bit synchronous up counter
2. Make K-maps from this table
3. Design your circuit from the results obtained in step 2
4. Simulate your circuit on ORCAD, make comments on the output, is it what you have expected?
5. **Design a 4 bit synchronous down counter by using T flip flops**

**Procedure:**

1. Fill the state transition table for a 3 bit synchronous down counter,
2. Make K-maps from this table,
3. Design your circuit from the results obtained in step 2,
4. Simulate your circuit on ORCAD, make comments on the output, is it what you have expected?
5. **BONUS**

Design a synchronous counter with a counting sequence 000, 001, 011, 111, 110, 100 and repeat.