**ECE 329**

**Digital Circuit Design II + Lab.**

**Fall 2018/2019**

**LAB # 5**

 **22.10.2018**

**Objective:**

To learn about asynchronous counters

1. **Using T Flip Flops in Design**
2. **Designing Synchronous Counters**
3. **Using External Inputs in Counter Design**
4. **Design a 3 bit synchronous up/down counter with an input x by using T flip flops, while x= 0 counter counts downward, otherwise (x=1) counter counts upward**

**Procedure:**

1. Fill the state transition table for a 3 bit synchronous up/down counter
2. Make K-maps from this table
3. Design your circuit from the results obtained in step 2
4. Simulate your circuit on ORCAD, make comments on the output, is it what you have expected?
5. **Design the circuit of Figure 1 on ORCAD and accomplish the following tasks.**

**Tasks:**

1. Understand the circuit’s working principle
2. Modify the circuit to count the sequence of 0,1,2,3,4,5,6,7,8,9,8,7,6,5,4,3,2,1,0,15,14,13,12,11,10,9,10,11,12,13,14,15,0, …
3. Now, modify the circuit once more to count a new sequence of 0.1.2.3.4.5.6.7.8.9.8,7,6,5,4.3,2,1,0,1,2…..

SHOW ALL YOUR WORK!

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FIGURE -1