**ECE 329**

**Digital Circuit Design II + Lab.**

**Fall 2018/2019**

**LAB # 6**

 **11.12.2018**

**Objective:**

To learn about shift register

1. **Using D Flip Flops in Design**
2. **Designing Shift Registers**
3. **Designing Full Adder**
4. **Design a 4 bit Shift Register (By using D Flip Flops)**

**Procedure:**

1. If possible use digstim (DIGSTIM ) as input, if not use digclock (DIGCLOCK).
2. Arrange your clock frequency well to avoid or minimize propagation delay.
3. **Design a full adder**

**Tasks:**

1. Understand the circuit’s working principle and fill the truth table below.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Cin | A | B | Sum | Cout |
| 0 | 0 | 0 |  |  |
| 0 | 0 | 1 |  |  |
| 0 | 1 | 0 |  |  |
| 0 | 1 | 1 |  |  |
| 1 | 0 | 0 |  |  |
| 1 | 0 | 1 |  |  |
| 1 | 1 | 0 |  |  |
| 1 | 1 | 1 |  |  |

1. Make K-maps from this table
2. Design your circuit from the results obtained in step 2
3. Simulate your circuit on ORCAD, make comments on the output, is it what you have expected?