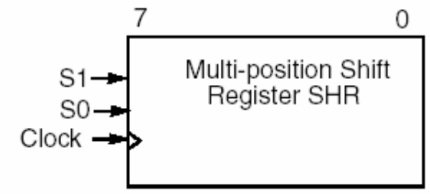
ECE 329 Final Preparation Questions

Q1. A company develops a custom shift register. The new register operates according to a 2-bit code (S1, S0) with the operations listed in the table below.



S1	S0	Operation
0	0	Rotate Right 1 Position
0	1	Rotate Right 2 Positions
1	0	Shift Left 1 Position
1	1	Shift Left 2 Positions

With the right rotate codes, the leftmost bits are filled with the bits falling out on the right, e.g., for a right rotates of 2 positions, 01110010 become 10011100.
With the left shiftcodes, the vacated rightmost bits are filled with 1's.

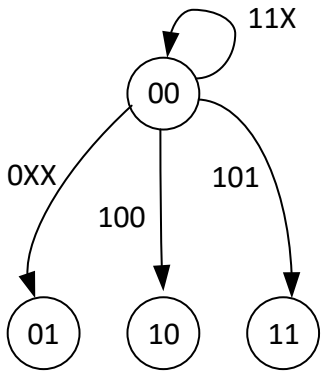
Manually simulate the register for 8 clock cycles with the initial contents and inputs as given in the simulation table below. The results due to any given line of the table are to appear on the following line due to the positive clock edge triggering of the register.

Clock Cycle	S1	S0	Shift Register Contents							
			7	6	5	4	3	2	1	0
1	1	1	0	0	0	1	0	1	0	0
2	0	1								
3	1	0								
4	0	0								
5	1	1								
6	0	0								
7	1	0								
8	0	1								

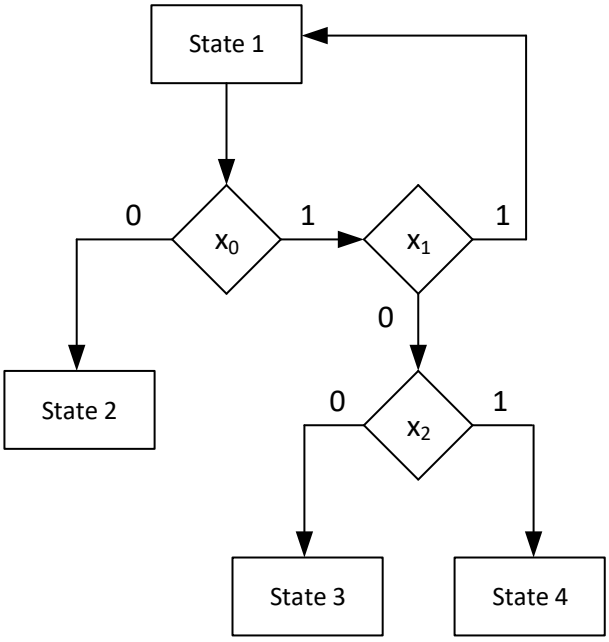
Solution:

Clock Cycle	S1	S0	Shift Register Contents							
			7	6	5	4	3	2	1	0
1	1	1	0	0	0	1	0	1	0	0
2	0	1	0	1	0	1	0	0	1	1
3	1	0	1	1	0	1	0	1	0	0
4	0	0	1	0	1	0	1	0	0	1
5	1	1	1	1	0	1	0	1	0	0
6	0	0	0	1	0	1	0	0	1	1
7	1	0	1	0	1	0	1	0	0	1
8	0	1	0	1	0	1	0	0	1	1
			1	1	0	1	0	1	0	0

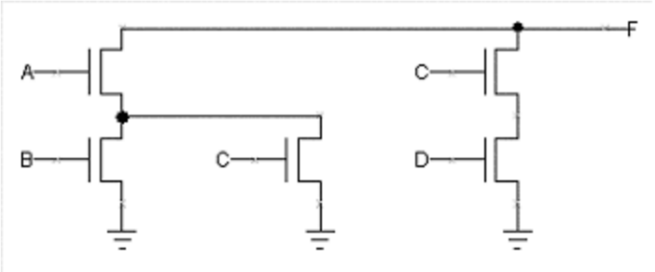
Q2. Draw the ASM chart equivalent to the State Diagram below



Solution:

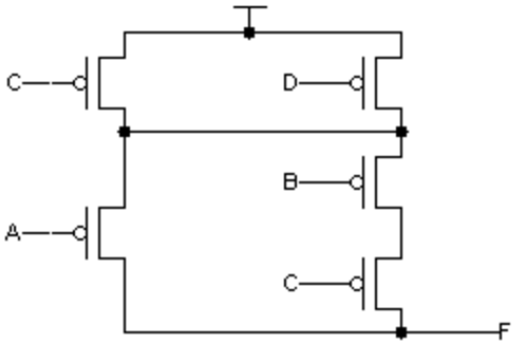


Q3. The pulldown circuit for a static CMOS logic gate that implements a certain function F(A,B,C,D) is given below.



a) Draw the corresponding pullup circuit.
b) Assuming the correct pullup circuitry is added to the diagram above, give a minimal sum-of-products expression for F(A,B,C,D).

Solution:
a)



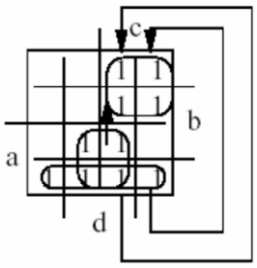
b) F= A(B+C)+CD = AB+AC+CD
or
F=(C'+D')(A'+B'C')=A'C'+A'D'+B'C'+B'C'D'=A'C'+A'D'+B'C'

Q4. We have a combinational circuit that implements the function:

F= A'C + AD + AB'

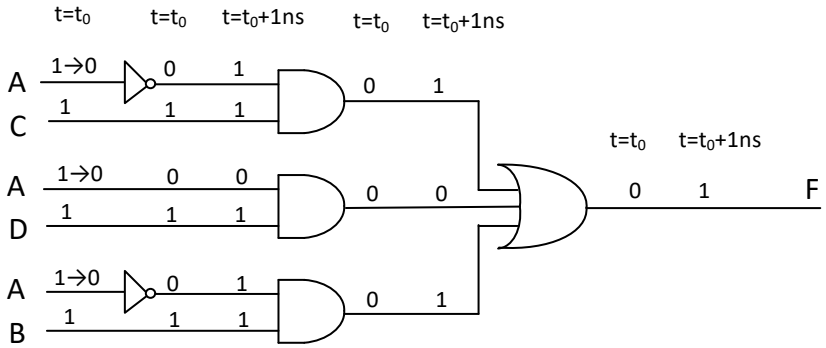
The circuit is a two-level AND-OR circuit with inverters at the input to generate A' and B'. All gates and inverters have a delay of 1ns. Can a single input change cause a static-1 hazard in this circuit? If yes, identify a single input change that causes a static-1 hazard. Use a Karnaugh map to demonstrate the static-1 hazard you have identified.

Solution:
Yes



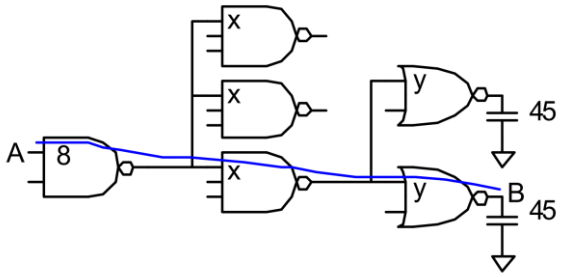
Further explanation:
The circuit is given below. Let's look at the terms A'C and AD. Check the Karnaugh map. These terms are not "connected". Now assume a change in input from 1111 to 0111 as the arrow in the middle of the given Karnaugh map indicates.

Before the input change the output is 1.
Since there is a 1ns delay for each gate, the outputs of the inverters will change from 0 to 1, 1 ns later. This will delay the change in the inputs of the top and bottom and gates. However, the input at the middle and gate will change at $t=t_0$ (no inverter). Therefore, at $t=t_0$, the inputs at the and gates are 01, 01 and 01.
This causes output to change to 0 for 1ns.
Then the output becomes 1 again.



All other indicated arrows on the Karnaugh map cause similar hazards.

Q5. For the multistage network given below, the PUN/PDN sizing for an inverter is given as 1/2. Evaluate the sizing factor for 2nd and 3rd stages (show all the steps in details).



Solution:

Logical Effort $G = g_1 g_2 g_3 = \frac{4}{3}\frac{5}{3}\frac{5}{3} = \frac{100}{27}$

Electrical Effort $F = \frac{C_{out}}{C_{in}} = \frac{45}{8}$

Branching Effort $B = b_1 b_2 = \frac{(C_{onpath1}+C_{offpath1})}{C_{onpath1}} \times \frac{(C_{onpath2}+C_{offpath2})}{C_{onpath2}} = \frac{C_1+3C_1}{C_1} \times \frac{C_2+2C_2}{C_2} = 3 \cdot 2 = 6$

Path Effort $H = \text{GBF} = \frac{100}{27} \cdot \frac{45}{8} \cdot 6 = 125$

Best stage effort $h = \sqrt[N]{H} = \sqrt[3]{125} = 5$

Work backward for sizes

$$h = 5 = g_3 b_3 f_3 = \frac{5}{3} \cdot 1 \cdot f_3 = \frac{5}{3} \cdot 1 \cdot \frac{45}{y} \quad \Rightarrow \quad y = \frac{45}{5} \cdot \frac{5}{3} = 15$$

$$h = 5 = g_2 b_2 f_2 = \frac{5}{3} \cdot 2 \cdot f_2 = \frac{5}{3} \cdot 2 \cdot \frac{15}{x} \quad \Rightarrow \quad x = \frac{15 \cdot 2}{5} \cdot \frac{5}{3} = 10$$

Check by making sure the sizing of the first stage matches our calculations:

$$h \overset{?}{=} 5 = g_1 b_1 f_1 \overset{?}{=} \frac{4}{3} \cdot 3 \cdot f_1 = \frac{4}{3} \cdot 3 \cdot \frac{10}{8} \quad \Rightarrow \quad 5 = 5 \ \surd$$